What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A method for measuring a parameter of a circuit under test, the method comprising:

(a) charging a test circuit with a power source;

(b) disconnecting said test circuit from said power source; and

(c) measuring said parameter of said circuit under test with said test circuit.

2. The method of claim 1, wherein said act of charging comprises:

charging a first portion of said test circuit up to a first voltage level; and

charging a second portion of said test circuit up to a second voltage level.

3. The method of claim 2, wherein said act of charging a first portion comprises charging a first capacitor of said test circuit to a power rail voltage level, and wherein said act of charging a second portion comprises charging a second capacitor of said test circuit to a predetermined reference voltage level.

4. The method of claim 3, wherein said act of charging a first capacitor comprises charging said first capacitor to Vdd.

5. The method of claim 3, wherein said act of charging a second capacitor comprises charging said second capacitor to an initial reference voltage level.

6. The method of claim 3 further comprising:

changing said predetermined reference voltage level; and

repeating acts (a) through (c) if said measured parameter does not have a predetermined relationship with said predetermined reference voltage level.

7. The method of claim 6, wherein said act of changing said predetermined reference voltage comprises changing said reference voltage level from an initial reference voltage level.

8. The method of claim 6, wherein said act of repeating comprises repeating acts (a) through (c) if a measured voltage is not less than said predetermined reference voltage level.

9. The method of claim 8, wherein said act of repeating comprises repeating acts (a) through (c) if a voltage measured at a ground terminal is not less than said predetermined reference voltage level.

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10. The method of claim 6, wherein said act of repeating comprises repeating acts (a) through (c) if a measured voltage is not less than said predetermined reference voltage level.

11. The method of claim 10, wherein said act of repeating comprises repeating acts (a) through (c) if a voltage measured at a power rail of said circuit under test is not less than said predetermined reference voltage level.

12. The method of claim 1, wherein said act of disconnecting comprises disconnecting said test circuit from a power rail of said circuit under test.

13. The method of claim 12, wherein said act of disconnecting comprises disconnecting said test circuit from a Vdd terminal.

14. The method of claim 12, wherein said act of disconnecting comprises disconnecting said test circuit from a reference voltage terminal.

15. The method of claim 13, wherein said act of disconnecting comprises toggling a state of a transistor coupled between said test circuit and said Vdd terminal.

16. The method of claim 14, wherein said act of disconnecting comprises toggling a state of a transistor coupled between said test circuit and said reference voltage terminal.

17. The method of claim 1, wherein said act of measuring comprises comparing a sensed voltage with a reference voltage.

18. The method of claim 17, wherein said act of comparing comprises comparing a voltage sensed at a ground terminal of said circuit under test with a reference voltage.

19. The method of claim 17, wherein said act of comparing comprises comparing a voltage sensed at a power rail of said circuit under test with a reference voltage.

20. The method of claim 18, wherein said act of comparing comprises toggling a state of a transistor coupled between the test circuit and said ground terminal being sensed.

21. The method of claim 19, wherein said act of comparing comprises toggling a state of a transistor coupled between the test circuit and said power rail being sensed.

22. The method of claim 1 further comprising quantifying ground bounce for said circuit under test.

23. The method of claim 1 further comprising quantifying power droop for said circuit under test.

24. A test circuit for measuring a parameter of a circuit under test, said test circuit comprising:

a charge retainer for retaining a charge from a power source for operating said test circuit;

a switch coupled between said charge retainer and said power source for disconnecting said test circuit from said power source; and

a measuring portion for measuring a parameter of said circuit under test while said test circuit is disconnected from said power source.

25. The test circuit of claim 24, wherein said charge retainer comprises a storage capacitor for storing a charge from said power source.

26. The test circuit of claim 25, wherein said switch comprises a transistor, a first side of said transistor being coupled to said storage capacitor, a second side of said transistor being coupled to said power source.

27. The test circuit of claim 24, wherein said measuring portion comprises a comparator, said comparator being coupled to said charge retainer for receiving power when said test circuit is disconnected from said power source.

28. The test circuit of claim 27, wherein a first input of said comparator is coupled to said circuit under test for sensing said parameter.

29. The test circuit of claim 28 further comprising a switch coupled between said first input of said comparator and said circuit under test.

30. The test circuit of claim 29, wherein said switch comprises a transistor.

31. The test circuit of claim 28, wherein a second input of said comparator is coupled to a reference voltage terminal for receiving a reference voltage and comparing said reference voltage with said sensed parameter of said circuit under test.

32. The test circuit of claim 31 further comprising a switch coupled between said second input of said comparator and said reference voltage terminal for disconnecting said second input of said comparator from said reference voltage terminal.

33. The test circuit of claim 32, wherein said switch comprises a transistor.

34. The test circuit of claim 32 further comprising a second charge retainer for retaining a charge from said reference voltage terminal.

35. The test circuit of claim 34, wherein said second charge retainer comprises a second storage capacitor for providing said reference voltage to said second input of said comparator when said second input is disconnected from said reference voltage terminal.

36. The test circuit of claim 27, wherein said comparator further comprises an output for producing a signal when said parameter, as measured, has a predetermined relationship with a reference voltage.

37. The test circuit of claim 24, wherein said test circuit is integrated onto a semiconductor die.

38. A semiconductor die comprising:

at least one circuit to be tested; and

at least one test circuit for measuring a parameter of said at least one circuit to be tested, said at least one test circuit comprising:

a charge retainer for retaining a charge from a power source for operating said at least one test circuit;

a switch coupled between said charge retainer and said power source for disconnecting said at least one test circuit from said power source; and

a measuring portion for measuring said parameter of said at least one circuit to be tested while said at least one test circuit is disconnected from said power source.

39. The die of claim 38, wherein said charge retainer comprises a storage capacitor for storing a charge from said power source.

40. The die of claim 39, wherein said switch comprises a transistor, a first terminal of said transistor being coupled to said storage capacitor, a second terminal of said transistor being coupled to said power source.

41. The die of claim 38, wherein said measuring portion comprises a comparator, said comparator being coupled to said charge retainer for receiving power when said at least one test circuit is disconnected from said power source.

42. The die of claim 41, wherein a first input of said comparator is coupled to said at least one circuit to be tested for sensing said parameter.

43. The die of claim 42 further comprising a switch coupled between said first input of said comparator and said at least one circuit to be tested.

44. The die of claim 43, wherein said switch comprises a transistor.

45. The die of claim 42, wherein a second input of said comparator is coupled to a reference voltage terminal for receiving a reference voltage and comparing said reference voltage with said sensed parameter of said at least one circuit to be tested.

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46. The die of claim 45 further comprising a switch coupled between said second input of said comparator and said reference voltage terminal for disconnecting said second input of said comparator from said reference voltage terminal.

47. The die of claim 46, wherein said switch comprises a transistor.

48. The die of claim 46 further comprising a second charge retainer for retaining a charge from said reference voltage terminal.

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49. The die of claim 48, wherein said second charge retainer comprises a second storage capacitor for providing said reference voltage to said second input when said second input is disconnected from said reference voltage terminal.

50. The die of claim 38, wherein said comparator further comprises an output for producing a signal when said parameter, as measured, has a predetermined relationship with a reference voltage.

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51. A semiconductor die comprising:

at least one circuit to be tested; and

at least one test circuit for measuring a parameter of said at least one circuit to be tested, said at least one test circuit comprising:

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a comparator coupled to a power source, said comparator having a first input for receiving a sensed voltage and a second input for receiving a reference voltage;

a first storage capacitor coupled to said voltage source and also coupled to said comparator, said first storage capacitor being used for storing a voltage supplied by said power source and also for providing power to said comparator when said comparator is disconnected from said power source;

a second storage capacitor coupled to a reference voltage source and also coupled to said second input of said comparator, said second storage capacitor being used for storing a reference voltage provided by said reference voltage source and also for providing said second input of said comparator with said reference voltage when said comparator is disconnected from said reference voltage source.

52. The die of claim 51 further comprising:

a first transistor coupled between said first input of said comparator and said at least one circuit to be tested for toggling said comparator in and out of electrical contact with said at least one circuit to be tested;

a second transistor coupled between said second input of said comparator and said reference voltage source for toggling said comparator in and out of electrical contact with said reference voltage source;

a third transistor coupled between said comparator and said power source for toggling said comparator in and out of electrical contact with said power source.

53. A computer readable storage medium storing a computer readable program for measuring a parameter of a circuit under test, said computer readable program being configured to operate a computer to:

(a) charge a test circuit with a power source;

(b) disconnect said test circuit from said power source; and

(c) measure said parameter of said circuit under test with said test circuit.

54. The storage medium of claim 53, wherein said program is further configured to operate said computer to:

charge a first portion of said test circuit up to a first voltage level; and

charge a second portion of said test circuit up to a second voltage level.

55. The storage medium of claim 54, wherein said program is further configured to operate said computer to charge a first capacitor of said test circuit to a power rail voltage level, and also to charge a second portion comprises charging a second capacitor of said test circuit to a predetermined reference voltage level.

56. The storage medium of claim 55, wherein said program is further configured to operate said computer to charge said first capacitor to Vdd.

57. The storage medium of claim 55, wherein said program is further configured to operate said computer to charge said second capacitor to an initial reference voltage level.

58. The storage medium of claim 55, wherein said program is further configured to operate said computer to:

change said predetermined reference voltage level; and

repeat acts (a) through (c) if said measured parameter does not have a predetermined relationship with said predetermined reference voltage level.

59. The storage medium of claim 58, wherein said program is further configured to operate said computer to change said reference voltage level from an initial reference voltage level.

60. The storage medium of claim 58, wherein said program is further configured to operate said computer to repeat acts (a) through (c) if a measured voltage is not less than said predetermined reference voltage level.

61. The storage medium of claim 60, wherein said program is further configured to operate said computer to repeat acts (a) through (c) if a voltage measured at a ground terminal is not less than said predetermined reference voltage level.

62. The storage medium of claim 58, wherein said program is further configured to operate said computer to repeat acts (a) through (c) if a measured voltage is not less than said predetermined reference voltage level.

63. The storage medium of claim 62, wherein said program is further configured to operate said computer to repeat acts (a) through (c) if a voltage measured at a power rail of said circuit under test is not less than said predetermined reference voltage level.

64. The storage medium of claim 53, wherein said program is further configured to operate said computer to disconnect said test circuit from a power rail of said circuit under test.

65. The storage medium of claim 64, wherein said program is further configured to operate said computer to disconnect said test circuit from a Vdd terminal.

66. The storage medium of claim 64, wherein said program is further configured to operate said computer to disconnect said test circuit from a reference voltage terminal.

67. The storage medium of claim 65, wherein said program is further configured to operate said computer to toggle a state of a transistor coupled between said test circuit and said Vdd terminal.

68. The storage medium of claim 66, wherein said program is further configured to operate said computer to toggle a state of a transistor coupled between said test circuit and said reference voltage terminal.

69. The storage medium of claim 53, wherein said program is further configured to operate said computer to compare a sensed voltage with a reference voltage.

70. The storage medium of claim 69, wherein said program is further configured to operate said computer to compare a voltage sensed at a ground terminal of said circuit under test with a reference voltage.

71. The storage medium of claim 69, wherein said program is further configured to operate said computer to compare a voltage sensed at a power rail of said circuit under test with a reference voltage.

72. The storage medium of claim 70, wherein said program is further configured to operate said computer to toggle a state of a transistor coupled between the test circuit and said ground terminal being sensed.

73. The storage medium of claim 71, wherein said program is further configured to operate said computer to toggle a state of a transistor coupled between the test circuit and said power rail being sensed.

74. The storage medium of claim 53, wherein said program is further configured to operate said computer to quantify ground bounce for said circuit under test.

75. The storage medium of claim 53, wherein said program is further configured to operate said computer to quantify power droop of said circuit under test.

76. A processor system, comprising:

a processor; and

a communications link coupled to said processor and also coupled to a computer readable storage medium, wherein

said computer readable storage medium stores a computer program for measuring a parameter of a circuit under test, said computer program configured to operate said processor to:

(a) charge a test circuit with a power source;

(b) disconnect said test circuit from said power source; and

(c) measure said parameter of said circuit under test with said test circuit.

77. The processor system of 76, wherein said program is further configured to operate said processor to:

charge a first portion of said test circuit up to a first voltage level; and

charge a second portion of said test circuit up to a second voltage level.

78. The processor system of claim 77, wherein said program is further configured to operate said processor to charge a first capacitor of said test circuit to a power rail voltage

level, and also to charge a second capacitor of said test circuit to a predetermined reference voltage level.

79. The processor system of claim 78, wherein said program is further configured to operate said processor to charge said first capacitor to Vdd.

80. The processor system of claim 78, wherein said program is further configured to operate said processor to charge said second capacitor to an initial reference voltage level.

81. The processor system of claim 78, wherein said program is further configured to operate said processor to:

change said predetermined reference voltage level; and

repeat acts (a) through (c) if said measured parameter does not have a predetermined relationship with said predetermined reference voltage level.

82. The processor system of claim 81, wherein said program is further configured to operate said processor to change said reference voltage level from an initial reference voltage level.

83. The processor system of claim 81, wherein said program is further configured to operate said processor to repeat acts (a) through (c) if a measured voltage is not less than said predetermined reference voltage level.

84. The processor system of claim 83, wherein said program is further configured to operate said processor to repeat acts (a) through (c) if a voltage measured at a ground terminal is not less than said predetermined reference voltage level.

85. The processor system of claim 81, wherein said program is further configured to operate said processor to repeat acts (a) through (c) if a measured voltage is not less than said predetermined reference voltage level.

86. The processor system of claim 85, wherein said program is further configured to operate said processor to repeat acts (a) through (c) if a voltage measured at a power rail of said circuit under test is not less than said predetermined reference voltage level.

87. The processor system of claim 76, wherein said program is further configured to operate said processor to disconnect said test circuit from a power rail of said circuit under test.

88. The processor system of claim 87, wherein said program is further configured to operate said processor to disconnect said test circuit from a Vdd terminal.

89. The processor system of claim 87, wherein said program is further configured to operate said processor to disconnect said test circuit from a reference voltage terminal.

90. The processor system of claim 88, wherein said program is further configured to operate said processor to toggle a state of a transistor coupled between said test circuit and said Vdd terminal.

91. The processor system of claim 89, wherein said program is further configured to operate said processor to toggle a state of a transistor coupled between said test circuit and said reference voltage terminal.

92. The processor system of claim 76, wherein said program is further configured to operate said processor to compare a sensed voltage with a reference voltage.

93. The processor system of claim 92, wherein said program is further configured to operate said processor to compare a voltage sensed at a ground terminal of said circuit under test with a reference voltage.

94. The processor system of claim 92, wherein said program is further configured to operate said processor to compare a voltage sensed at a power rail of said circuit under test with a reference voltage.

95. The processor system of claim 93, wherein said program is further configured to operate said processor to toggle a state of a transistor coupled between the test circuit and said ground terminal being sensed.

96. The processor system of claim 94, wherein said program is further configured to operate said processor to toggle a state of a transistor coupled between the test circuit and said power rail being sensed.

97. The processor system of claim 76, wherein said program is further configured to operate said processor to quantify ground bounce for said circuit under test.

98. The processor system of claim 76, wherein said program is further configured to operate said processor to quantify power droop of said circuit under test.